UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/905,195	07/16/2001	Nobuaki Shinmori	KAN 135	3051

23995 7590 10/26/2005

RABIN & Berdo, PC
1101 14TH STREET, NW
SUITE 500
WASHINGTON, DC 20005

EXAMINER	
DUNCAN, MARC M	

ART UNIT	PAPER NUMBER
2113	

DATE MAILED: 10/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/905,195	SHINMORI, NOBUAKI	
	Examiner	Art Unit	
	Marc Duncan	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-3* is/are allowed.

6)☒ Claim(s) *4 and 8* is/are rejected.

7)☒ Claim(s) *5-7,9 and 10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

FINAL REJECTION

Status of the Claims

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iwata et al. (6,662,314) in view of Mayer (6,769,065).

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iwata and Mayer as applied to claim 8 above, and further in view of Grimmer, Jr. et al. (5,737,760).

Claims 1-3 are allowed.

Claims 5-7 and 9-10 are objected to.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iwata et al. (6,662,314) in view of Mayer (6,769,065).

Regarding claim 8:

Iwata teaches a memory device to store a control program, data and a security bit in col. 1 lines 60-64, col. 18 lines 42-46 and col. 25 lines 48-53.

Iwata teaches a central processing unit to execute a specific process according to the program in col. 2 lines 41-46 and col. 6 lines 5-24.

Iwata teaches a test port to input and output test signals in col. 5 lines 63-66.

Iwata teaches controlling on/off between the test port and the central processing unit in col. 1 line 64-col. 2 line 5 and col. 4 line 64-col. 5 line 6.

Iwata teaches controlling the on/off if the security bit has been changed to a predetermined state and based on a match of input data with data stored in the memory device in col. 18 line 47-col. 19 line 10.

Iwata does not explicitly teach a switch controlling the on/off. Iwata does not explicitly teach security control means for selectively turning off the switch and for comparing data input via the test port with the data stored in the memory and turning on the switch when the data agree. Iwata does, however, teach controlling the on/off if the security bit has been changed to a predetermined state and based on a match of input data with data stored in the memory device in col. 18 line 47-col. 19 line 10.

Mayer teaches a switch controlling the on/off in col. 4 lines 43-48. The inhibit signal controls the access authorization circuit to act as a switch. In one state the circuit is on and the data access is allowed. In the opposite state, the data flow is cut off.

Mayer also teaches comparing data input via the test port with the data stored in the memory and turning on the switch when the data agree in col. 4 lines 32-42.

It would have been obvious to one of ordinary skill in the art at the time of invention to combine the teachings of Iwata with the switch function of Mayer.

One of ordinary skill in the art at the time of invention would have been motivated to make the combination because Mayer discloses that the use of such a system allows

the risk of misuse of the JTAG interface to be kept to a minimum and allows for greater security of internal registers and memories of a circuit.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iwata and Mayer as applied to claim 8 above, and further in view of Grimmer, Jr. et al. (5,737,760).

Regarding claim 4:

Iwata teaches a memory device to store a control program and data, the data stored in the memory device including said first data in col. 1 lines 60-64, col. 18 lines 42-46 and col. 25 lines 48-53.

Iwata teaches a central processing unit to execute a specific process according to the program in col. 2 lines 41-46 and col. 6 lines 5-24.

Iwata teaches storing second data, said second data including a security bit in col. 1 lines 60-64, col. 18 lines 42-46 and col. 25 lines 48-53.

Iwata teaches a test port to input and output test signals, including said first data in col. 5 lines 63-66 and col. 18 lines 42-46.

Iwata teaches controlling the on/off between the test port and at least one of the memory device and the central processing unit according to the security bit in col. 18 line 47-col. 19 line 10.

Iwata does not explicitly teach a switch controlling the on/off. Iwata does, however, teach controlling the on/off between the test port and at least one of the memory device and the central processing unit according to the security bit in col. 18 line 47-col. 19 line 10.

Mayer teaches a switch controlling the on/off in col. 4 lines 43-48. The inhibit signal controls the access authorization circuit to act as a switch. In one state the circuit is on and the data access is allowed. In the opposite state, the data flow is cut off.

It would have been obvious to one of ordinary skill in the art at the time of invention to combine the teachings of Iwata with the switch function of Mayer.

One of ordinary skill in the art at the time of invention would have been motivated to make the combination because Mayer discloses that the use of such a system allows the risk of misuse of the JTAG interface to be kept to a minimum and allows for greater security of internal registers and memories of a circuit.

Iwata and Mayer do not explicitly teach the second data including a security bit being stored in a non-volatile register. Iwata and Mayer do, however, teach the second data including a security bit being stored in a non-volatile memory.

Grimmer teaches storing a security bit in a non-volatile register in the Abstract lines 16-17.

It would have been obvious to one of ordinary skill in the art at the time of invention to combine the security bit storage of Iwata and Mayer with the non-volatile register of Grimmer.

One of ordinary skill in the art at the time of invention would have been motivated to make the combination because storing the second data including the security bit in a non-volatile register allows the security data to be stored permanently without using additional memory space.

Allowable Subject Matter

Claims 5-7 and 9-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: Prior art was not found that explicitly teaches or fairly suggests allowing or preventing communication of signals between the JTAG port and the TAP depending on the state of the security bit as outlined in claim 1. The reasons for indicating allowability of claims 5-7 and 9-10 are addressed in the previous office action.

Response to Arguments

Applicant's arguments filed 8/8/05 have been fully considered but they are not persuasive.

Regarding applicant's arguments concerning the security bit of claims 4 and 8, the examiner respectfully disagrees. Applicant is correct in stating that the security level bit of Iwata corresponds to the security bit of the instant claims. Applicant, however, further states that the reference does not appear to express the location of the security bit. The examiner would like to point out the citation to col. 25 lines 48-53, in which the reference states the location of the security bit in a particular embodiment as in the flash memory device.

Regarding applicant's argument that the cited passages do not support the contention that Iwata controls on/off between the test port and the CPU, the examiner

respectfully disagrees. Iwata teaches disabling all abilities of the debug tool. In other words, the debugging tool is not allowed to communicate with the circuit until it has been reset. Hence, on/off is controlled between the test port and the CPU. Applicant correctly states that Iwata does not disclose a switch as in claim 8. The examiner did not point to Iwata to disclose a switch. The examiner admits the switch was not disclosed in Iwata and therefore made a proper combination with the Mayer reference to show the obviousness of the switch.

Regarding applicant's argument that Iwata does not teach controlling the on/off according to the security bit, the examiner respectfully disagrees. As applicant correctly states, Iwata teaches controlling on/off based on the bit when the security codes do not match. It is clear, then, that the claims read on this situation in that there is a period of time when the function of the debug tool is limited based on the security bit and this limitation of the tool from communicating with the circuit components corresponds to the on/off teaching of the claims. Applicant submits a hypothetical situation in which the security level bit of Iwata is inconsequential to the on/off function. While the examiner does not necessarily disagree, the examiner reminds applicant that a single hypothetical situation illustrating the alleged benefits of the instant claimed invention does not obviate the rejection. The Iwata reference teaches a situation in which the security bit is the deciding factor in the on/off situation of the test port and thus is read on by the broad, reasonably interpreted language of the claims. The examiner would further like to note applicant's claim 5, in which a logic gate turns on the switch when data from a memory device and input data agree, independent of the security bit. The examiner

submits that this is clearly equivalent to the situation described by the Iwata reference in which, when a security code is matched to a stored security code, the debugging tool is allowed to function regardless of security level.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Marc Duncan whose telephone number is 571-272-3646. The examiner can normally be reached on M-F 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on 571-272-3645. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

md

ROBERT BEAUSOLIEL
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100